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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,462	11/21/2001	Han Kyoung Cho	K-0348	1697

34610 7590 10/31/2006

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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,462	CHO, HAN KYOUNG	
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-14 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-14 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed Aug. 15, 2006 have been fully considered but they are not persuasive.

In re page 2, applicant states that the failure of the examiner in addressing arguments submitted by applicant against the rejections in applicant's amendment filed October 3, 2005 does little to help further prosecution of the present application.

It is agreed that without addressing arguments against the rejections in applicant's amendment filed October 3, 2005 does little to help further prosecution of the present application. After reviewing the arguments filed Oct. 3, 2005, it is noted that the arguments filed Oct. 3, 2005 and the arguments filed Aug. 15, 2006 are similar.

In re pages 3-6, applicant argues that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of these claims of, inter alia, a given number of bits of the video signal from the second video process part being selected and presented in order of significance level thereof, superimposing a video signal by adding bits of the video signal from the first video processing part in reverse order of significance level thereof with the video signal bits presented from the adjusting part, or adding bits of a video signal of the main picture in reverse order of significance level thereof with bits of a video signal of the PIP selected and presented in order of significance level thereof according to the adjusted mix ratio.

In response, the examiner respectfully disagrees. Jenison discloses in the abstract that "the most significant bit down to the least significant bit of the digital control word is connected to the switches in the switch-ladder network to achieve the desired output, which is combination with the resistor ladder network, will achieve the desired combination of input video signals" and from col. 2, line 67 to col. 3, line 9 that "Therefore, half the total current is "steered" by switch 3 which is controlled by the most significant bit of the control word. One quarter of the total current is "steered" by switch 4 which is controlled by the second-most significant bit, bit 6 of the control work. The result is that the control word causes the switches to apply the proper combinations of video signal A and B to the resistor network in response to the desired digital control word, and in increasing and decreasing proportions corresponding to the increasing and decreasing value of the control word". From the above passages, it is noted that, by controlling the control word, either video signals A and B would be outputted in the reverse order of significance level there of. Thus, Jenison does indeed disclose the argued limitations.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7-9, 11-12 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainville et al. (Publication No. US2002/0069411A1) in view of Jenison (US Patent No. 5,175,623).

In considering claim 1, Rainville et al disclose all the claimed subject matter, note, 1) the claimed a device for processing a PIP (picture in picture) in a TV comprising: a first video processing part for receiving, and processing a main picture video signal into a signal displayable on a screen is met by the parsing and layout engine 206 which conditions the HTML data for display on a television screen and extracts the specific video related information from the HTML source 202 (Fig. 6, page 3, [0033]-[0036]), 2) the claimed a second video processing part for receiving, and processing a sub picture video signal into a signal displayable on a region of the screen is met by the video processor 210 for decoding the MPEG Audio/Video compressed stream 203 (Fig. 6, page 3, [0038]-[0039]), 3) the claimed a control part for providing a control signal according to a users command is met by the video and graphics (GFX) control engine 208 which takes the user inputs 201, which consist of Picture-In-Graphics (PIG) controls 205 and transparency controls 204 (Fig. 6, page 3, [0037]), 4) the claimed an adjusting part for adjusting a presenting ratio of a video signal from the second video processing part is met by the video and graphics (GFX) control engine 208 which takes the user inputs 201, which consist of Picture-In-Graphics (PIG) controls 205 and transparency controls 204 (Fig. 6, page 3, [0037]), and 5) the claimed a switching part for superimposing the video signal from the first video processing part and the video signal from the adjusting part according to the control signal from the

control part is met by the display formatter module 212 and the video resizing module 211 which allow flexible combinations of graphics data 215 and real time video stream data 216 to form a various Picture In Graphics (PIG) and transparency combinations at the output 213, as illustrated in Figs. 3A-3C, 4A, 4B and 5A-5E (Fig. 6, page 3, [0038] and page 4, [0058]-[0064]).

However, Rainville et al explicitly do not disclose the claimed wherein a given number of bits of the video signal from the second video processing part are selected and presented in order of significance level thereof, and by adding bits of the video signal from the first video processing part in reverse order of significance level thereof with the video signal bits presented from the adjusting part.

Jenison teaches that a linear video mixer with digital control comprised of two buffer means, whose inputs are connected to the two video signals to be mixed, each buffer means having a low output impedance and each output connected to alternative inputs of n electrically controlled double-throw switches... and where an n byte word provides the control signals for each of the n respective switches with **the most significant bit of the control word** connected to the switch control at one end of the switch ladder network with **the least significant bit** connected to the next switch control, and continuing on down accordingly to the opposing end of the switch-ladder network (Fig. 1, col. 1, line 56 to col. 3, line 38).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the mixing two video signal as taught by Jenison into Rainville et al' s system in order to produce a linear keyer which responds directly to

numerical control in binary form and uses this data to proportionally combine two video signals.

In considering claim 7, Rainville et al disclose all the claimed subject matter, note 1) the claimed a method for processing a PIP in a TV, comprising the steps of: displaying the PIP when a user selects a PIP function is met by Figs. 2A-2C, the combined PIP/background image (page 2, [0026]-[0028]), 2) the claimed displaying a mix ratio of the displayed PIP and main picture is met by Figs. 5A-5E which show different modes of operation based on viewer control over the size, position and degree of transparency (or level of translucency) of the Picture-In-Graphics (PIG) television video image (page 2, [0029]-[0032]), and 3) the claimed adjusting the mix ratio the user desires with reference to the displayed mix ratio is met by the display formatter module 212 and the video resizing module 211 which allow flexible combinations of graphics data 215 and real time video stream data 216 to form a various Picture In Graphics (PIG) and transparency combinations at the output 213, as illustrated in Figs. 3A-3C, 4A, 4B and 5A-5E (Fig. 6, page 3, [0038] and page 4, [0058]-[0064]).

However, Rainville et al explicitly do not disclose the claimed adding bits of a video signal of the main picture in reverse order of significance level thereof with bits of a video signal of the PIP selected and presented in order of significance level thereof according to the adjusted mix ratio.

Jenison teaches that a linear video mixer with digital control comprised of two buffer means, whose inputs are connected to the two video signals to be mixed, each buffer means having a low output impedance and each output connected to alternative

inputs of n electrically controlled double-throw switches... and where an n byte word provides the control signals for each of the n respective switches with the most significant bit of the control word connected to the switch control at one end of the switch ladder network with the least significant bit connected to the next switch control, and continuing on down accordingly to the opposing end of the switch-ladder network (Fig. 1, col. 1, line 56 to col. 3, line 38).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the mixing two video signal as taught by Jenison into Rainville et al' s system in order to produce a linear keyer which responds directly to numerical control in binary form and uses this data to proportionally combine two video signals.

In considering claim 8, the claimed wherein displaying the mix ratio includes displaying the mix ratio in a form of an OSD is met by Figs. 5A-5E which show different modes of operation based on viewer control over the size, position and degree of transparency (or level of translucency) of the Picture-In-Graphics (PIG) television video image (page 2, [0029]-[0032] of Rainville et al).

In considering claim 9, the claimed wherein adjusting the mix ratio includes adjusting a luminance of a PIP according to a users requirement with reference to the mix ratio displayed an OSD (On screen display) form, for adjusting the mix ratio of a picture in a region the main picture and the sub picture are superimposed is met by Figs. 5A-5E which show different modes of operation based on viewer control over the size, position and degree of transparency (or level of translucency) of the Picture-In-

Graphics (PIG) television video image because adjusting the weighted of each pixel in television video image means adjusting the luminance value of each pixel in television video image (page 2, [0029]-[0032] of Rainville et al).

In considering claim 11, Rainville et al. disclose all the claimed subject matter, note 1) the claimed a method for processing a PIP (picture in picture) in a digital television receiver, the method comprising: processing a first video signal representative of a main picture into main picture data displayable on a display screen is met by the parsing and layout engine 206 which conditions the HTML data for display on a television screen and extracts the specific video related information from the HTML source 202 (Fig. 6, page 3, [0033]-[0036]), 2) the claimed processing a second video signal representative of a sub picture into sub picture data displayable on a portion of the display screen is met by the video processor 210 for decoding the MPEG Audio/Video compressed stream 203 (Fig. 6, page 3, [0038]-[0039]), 3) the claimed outputting a given number of data bits among the sub picture data according to a user command in order of significant level thereof is met by the video and graphics (GFX) control engine 208 which takes the user inputs 201, which consist of Picture-In-Graphics (PIG) controls 205 and transparency controls 204 and the output from the video and graphics (GFX) control engine 208 should be the number of data bits because it operating in the digital domain (Fig. 6, page 3, [0037]), and 4) the claimed superimposing the outputted sub picture data bits on the main picture data is met by the display formatter module 212 and the video resizing module 211 which allow flexible combinations of graphics data 215 and real time video stream data 216 to form a

various Picture In Graphics (PIG) and transparency combinations at the output 213, as illustrated in Figs. 3A-3C, 4A, 4B and 5A-5E (Fig. 6, page 3, [0038] and page 4, [0058]-[0064]).

However, Rainville et al explicitly do not disclose the claimed wherein the outputted sub picture data bits are added to bits of the main picture data in reverse order of significance of the main picture data bits during the superimposing.

Jenison teaches that a linear video mixer with digital control comprised of two buffer means, whose inputs are connected to the two video signals to be mixed, each buffer means having a low output impedance and each output connected to alternative inputs of n electrically controlled double-throw switches... and where an n byte word provides the control signals for each of the n respective switches with the most significant bit of the control word connected to the switch control at one end of the switch ladder network with the least significant bit connected to the next switch control, and continuing on down accordingly to the opposing end of the switch-ladder network (Fig. 1, col. 1, line 56 to col. 3, line 38).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the mixing two video signal as taught by Jenison into Rainville et al' s system in order to produce a linear keyer which responds directly to numerical control in binary form and uses this data to proportionally combine two video signals.

In considering claim 12, the claimed further comprising displaying the added main picture data on the display screen, wherein both of the main and sub pictures are

viewable in the portion of the display screen is met by Figs. 3A-3C, the viewer has control over the transparency of the television video image 503, transparent (or translucent) television video image 503 is in the foreground, overlaid on Web page 500, by being transparent, television video image 503 does not obscure Web page 500 (page 2, [0027]-[0028] of Rainville et al).

In considering claim 17, Rainville et al. disclose all the claimed subject matter, note 1) the claimed a method for processing a PIP (picture in picture) in a digital television receiver, the method comprising: a first video processing unit processing a first video signal representative of a main picture into displayable main picture data is met by the parsing and layout engine 206 which conditions the HTML data for display on a television screen and extracts the specific video related information from the HTML source 202 (Fig. 6, page 3, [0033]-[0036]), 2) the claimed second video processing unit processing a second video signal representative of a sub picture into displayable sub picture data is met by the video processor 210 for decoding the MPEG Audio/Video compressed stream 203 (Fig. 6, page 3, [0038]-[0039]), 3) the claimed a controller generating a control signal according to a user command is met by the video and graphics (GFX) control engine 208 which takes the user inputs 201, which consist of Picture-In-Graphics (PIG) controls 205 and transparency controls 204 (Fig. 6, page 3, [0037]), 3) the claimed an output unit coupled to the controller for outputting a given number of data bits among the sub picture data in order of significance level thereof in response to the control signal is met by the output from the video and graphics (GFX) control engine 208 should be the number of data bits because it operates in the digital

domain (Fig. 6, page 3, [0037]), and 5) the claimed a switching unit coupled to the output unit for superimposing the outputted sub picture data bits on the main picture data is met by the display formatter module 212 and the video resizing module 211 which allow flexible combinations of graphics data 215 and real time video stream data 216 to form a various Picture In Graphics (PIG) and transparency combinations at the output 213, as illustrated in Figs. 3A-3C, 4A, 4B and 5A-5E (Fig. 6, page 3, [0038] and page 4, [0058]-[0064]).

However, Rainville et al explicitly do not disclose the claimed wherein the switching unit superimposes the outputted sub picture data bits on the main picture data by adding the outputted sub picture data bits with bits of the main picture data in reverse order of significance of the main picture data bits.

Jenison teaches that a linear video mixer with digital control comprised of two buffer means, whose inputs are connected to the two video signals to be mixed, each buffer means having a low output impedance and each output connected to alternative inputs of n electrically controlled double-throw switches...and where an n byte word provides the control signals for each of the n respective switches with the most significant bit of the control word connected to the switch control at one end of the switch ladder network with the least significant bit connected to the next switch control, and continuing on down accordingly to the opposing end of the switch-ladder network (Fig. 1, col. 1, line 56 to col. 3, line 38).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the mixing two video signal as taught by Jenison into

Rainville et al' s system in order to produce a linear keyer which responds directly to numerical control in binary form and uses this data to proportionally combine two video signals.

In considering claim 18, the claimed further comprising a display screen coupled to the switching unit for displaying the superimposed picture data, wherein both of the main and sub pictures are viewable in the portion of the display screen is met by the television 102 of Figs. 3A-3C, the viewer has control over the transparency of the television video image 503, transparent (or translucent) television video image 503 is in the foreground, overlaid on Web page 500, by being transparent, television video image 503 does not obscure Web page 500 (page 2, [0027]-[0028] of Rainville et al).

4. Claims 2-3, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainville et al. (Publication No. US2002/0069411A1) in view of Jenison (US Patent No. 5,175,623), and further in view of Yoo et al. (US Patent No. 6,333,762 B1).

In considering claim 2, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the first video processing part includes: an analog/ digital converter for receiving, and converting analog R, G, B video signals into digital R, G, B video signals, and a format converter for maintaining outputs of the digital R, G, B video signals converted at the analog/digital converter constant.

Yoo et al teach that referring to Fig. 10, an ADC & PLL (analog-to-digital converter and phase locked loop) 110 converts RGB signals input from a personal

computer or a set-top box to digital data... and meanwhile, the scan format converter 300 according to an embodiment of the present invention bi-sigmoid-interpolates 8-bit RGB signal levels input from the ADC & PLL 100 to convert them to the high or low resolution video format (col. 6, lines 1-48) and the output from the scan format converter 300 is maintain at 8-bits (Fig. 10).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the A/D converter and the scan format converter as taught by Yoo et al the combination of Rainville et al and Jenison's system in order to provide the scan format converter which can display various video formats (e.g., SVGA, XGA and VGA) input from the external device such as a personal computer or a set-top box on a display unit of the projection television or a home television, without degradation of the image quality (col. 10, lines 17-22 of Yoo et al).

In considering claim 3, Rainville et al disclose all the claimed subject matter, note 1) the claimed wherein the second video processing part includes: a video decoder for receiving a video signal, and decoding the sub picture video signal from the video signal is met by the video processor 210 for decoding the MPEG Audio/Video compressed stream 203 (Fig. 6, page 3, [0038]-[0039]). However, the combination of Rainville et al and Jenison explicitly do not disclose the claimed a second format converter for converting an output of the video signal decoded at the video decoder constant.

Yoo et al teach that referring to Fig. 10, the scan format converter 300 according to an embodiment of the present invention bi-sigmoid-interpolates 8-bit RGB signal levels input from the ADC & PLL 100 to convert them to the high or low resolution video

format (col. 6, lines 1-48) and the output from the scan format converter 300 is maintain at 8-bits (Fig. 10).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the scan format converter as taught by Yoo et al into the combination of Rainville et al and Jenison's system in order to provide the scan format converter which can display various video formats (e.g., SVGA, XGA and VGA) input from the external device such as a personal computer or a set-top box on a display unit of the projection television or a home television, without degradation of the image quality (col. 10, lines 17-22 of Yoo et al).

In considering claim 13, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 11 above, except for providing the claimed wherein the first video processing representative of a main picture includes: receiving analog R, G, and B video signals representative of the main picture and converting analog R, G, B video signals into digital R, G, B video signals, and converting a format of the converted digital R, G, B video signals into a required format.

Yoo et al teach that referring to Fig. 10, an ADC & PLL (analog-to-digital converter and phase locked loop) 110 converts RGB signals input from a personal computer or a set-top box to digital data... and meanwhile, the scan format converter 300 according to an embodiment of the present invention bi-sigmoid-interpolates 8-bit RGB signal levels input from the ADC & PLL 100 to convert them to the high or low resolution video format (col. 6, lines 1-48).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the A/D converter and the scan format converter as taught by Yoo et al into the combination of Rainville et al and Jenison's system in order to provide the scan format converter which can display various video formats (e.g., SVGA, XGA and VGA) input from the external device such as a personal computer or a set-top box on a display unit of the projection television or a home television, without degradation of the image quality (col. 10, lines 17-22 of Yoo et al).

Claim 19 is rejected for the same reason as discussed in claim 13.

5. Claims 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainville et al. (Publication No. US2002/0069411A1) in view of Jenison (US Patent No. 5,175,623), and further in view of Lee (US Patent No. 6,373,527 B1).

In considering claim 14, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 11 above, except for providing the claimed wherein the second video processing representative of a sub picture includes: receiving a composite video signal and extracting a video signal representative of the sub picture from the composite signal, and converting a format of the extracted video signal into a require format.

Lee teach that the A/V switch 41 in the NTSC analog broadcasting signal processor 40 outputs one of the NTSC analog broadcasting signals received from the IF module 32 and the external input port 20 to a chroma processor 42, the chroma processor 42 generates a luminance signal Y, a first color difference signal R-Y and a second color difference signal B-Y being the second image signal from the NTSC

analog broadcasting signal received from the A/V switch 41 and then outputs the generated signals to a second A/D converter 43 and outputs the A/D converted second image signal to a second format converter 62 in the format conversion portion 60, the format conversion portion 60 is a block for converting the frame formats of the first and second image signals respectively received from the HD digital broadcasting signal processor 30 and the NTSC analog broadcasting signal processor 40, into a predetermined frame format (Fig. 1, col. 3, line 41 to col. 4, line 18).

Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the video processor which includes the chroma processor and the format converter as taught by Lee into the combination of Rainville et al and Jenison's system in order to provide an HDTV for synthesizing a plurality of image signals contained in the broadcasting signals of mutually different broadcasting systems into a single picture-in-picture (PIP) image signal and displaying the synthesized PIP image signal on the screen (col. 1, line 65 to col. 2, line 2 of Lee).

Claim 20 is rejected for the same reason as discussed in claim 14.

6. Claims 4, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainville et al. (Publication No. US2002/0069411A1) in view of Jenison (US Patent No. 5,175,623), and further in view of Tsujimoto et al. (US Patent No. 5,625,764).

In considering claim 4, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the adjusting part is a bit shifter. Tsujimoto et al teach that the addition circuit 201 inputs 8-bit binary numbers which have been multiplied by

their respective weights (i.e., ½, ¼ 1/8, 1/16 and 1/16) **by means of digit shift**, sums those products and outputs a sum, these weights total to 1 and form a geometrical progression of a common ratio of ½, the weight of output is total of weights (i.e., 1) and is shifted 4 digit places from the minimum weight of 1/16, therefore, the outputs is 12 bits, the selectors 202-206 select between an INPUT SIGNAL A and an INPUT SIGNAL B for their respective weight inputs, S2-S6 are selector control signals (Figs. 30 and 31, col. 25, line 9 to col. 27, line 21). Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the addition circuit with digit shift as taught by Tsujimoto et al into the combination of Rainville et al and Jenison's system in order to correctly calculate the blending ratio to prevent the decrease of the brightness of the video signal to be displayed (col. 9, lines 24-28 of Tsujimoto et al).

In considering claim 10, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 7 above, except for providing the claimed wherein the step (c) includes the step of fixing the mix ratio depending on connections between the video signal data from the first video processing part and the video signal from the second video processing part according to a user's requirement. Tsujimoto et al teach that the addition circuit 201 inputs 8-bit binary numbers which have been multiplied by their respective weights (i.e., ½, ¼ 1/8, 1/16 and 1/16) **by means of digit shift**, sums those products and outputs a sum, these weights total to 1 and form a geometrical progression of a common ratio of ½, the weight of output is total of weights (i.e., 1) and is shifted 4 digit places from the minimum

weight of 1/16, therefore, the outputs is 12 bits, the selectors 202-206 select between an INPUT SIGNAL A and an INPUT SIGNAL B for their respective weight inputs, S2-S6 are selector control signals (Figs. 30 and 31, col. 25, line 9 to col. 27, line 21). Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the addition circuit with digit shift as taught by Tsujimoto et al into the combination of Rainville et al and Jenison's system in order to correctly calculate the blending ratio to prevent the decrease of the brightness of the video signal to be displayed (col. 9, lines 24-28 of Tsujimoto et al), since the selectors 202-206 select between an INPUT SIGNAL A and an INPUT SIGNAL B for their respective weight inputs, the ratio of Tsujimoto et al is fixed depending on connections between the video signal data from the first video processing part and the video signal from the second video processing part according to a users requirement.

In considering claim 15, the combination of Rainville et al and Jenison disclose all the limitations of the instant invention as discussed in claim 11 above, except for providing the claimed wherein the given number of sub picture data bits are selected in descending order of significance of bits. Tsujimoto et al teach that the pixel blend unit 104 blends these RGB pixel data according to a blend ratio that is supplied to the unit 104 in synchronization with the RGB pixel data supply thereby outputting the result of the blending operation, in the present embodiment, the blend ratio is represented by a 5-bit fixed-point binary number and its MSB represents units (descending order)...and A is the value of any one of RGB components output from the first image memory 102 (main picture), and B is the value of the same color component as above output from

the second image memory 103 (sub-picture), since each of RGB components are formed by 8 bits, decimal place values are rounded-down (Fig. 14, col. 19, lines 1-39). Therefore, it would have been obvious to one of ordinary skill in the art of the time of the invention to incorporate the number of bits in binary number and its MSB represent unit (descending order) as taught by Tsujimoto et al into the combination of Rainville et al and Jenison's system in order to correctly calculate the blending ratio to prevent the decrease of the brightness of the video signal to be displayed (col. 9, lines 24-28 of Tsujimoto et al).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 28, 2006

Trang U. Tran
Primary Examiner
Art Unit 2622